

A HIGH CMRR, LOW-POWER OPERATIONAL TRANSCONDUCTANCE AMPLIFIER WITH 0.18 μ M CMOS TECHNOLOGY

BHUPENDRA BANJARE, D. S. AJNAR & P. K. JAIN

Department of Electronics & Instrumentation Engineering, Shri G. S. Institute of Technology and Science, Indore,
Madhya Pradesh, India

ABSTRACT

This paper represent an Operational Transconductance Amplifier (OTA) which is a basic building block in many analog circuit such as in data converter's (ADC & DAC), biquad filter design and instrumentation amplifiers. This OTA is implemented using 0.18 μ m CMOS technology with cadence environment and it has ± 1.25 v power supply with biasing current of 33nA. OTA has been simulated with virtuoso simulator and simulation results are measured. Post layout simulations for a 1 pF load capacitance shows that OTA achieves a gain bandwidth of 270 KHz at a phase margin 68.43° with 90.27 dB DC gain. This OTA is having CMRR of 154 dB, PSRR of 119 dB, Power dissipation of 29.58nW and Slew Rate 2.49 V/ μ sec.

KEYWORDS: Cadence, Operational Transconductance Amplifier (OTA), CMRR, PSRR, DC Gain, Unity Gain Bandwidth (UGBW), CMFB